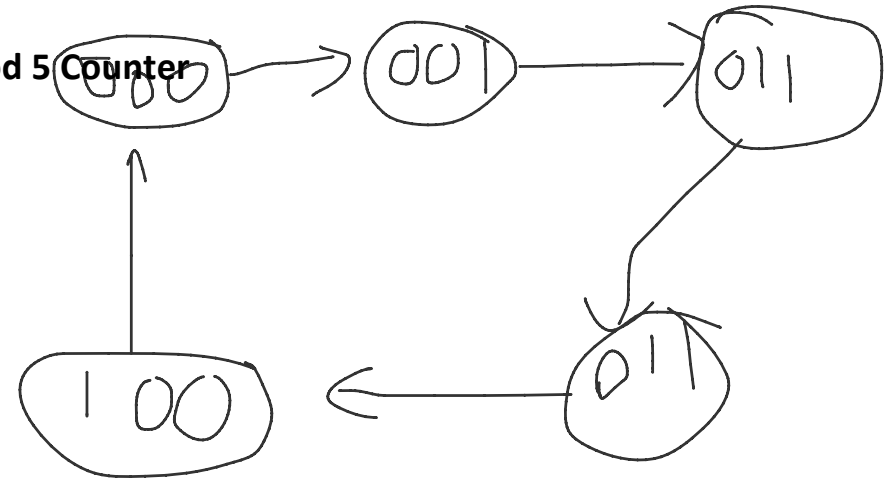
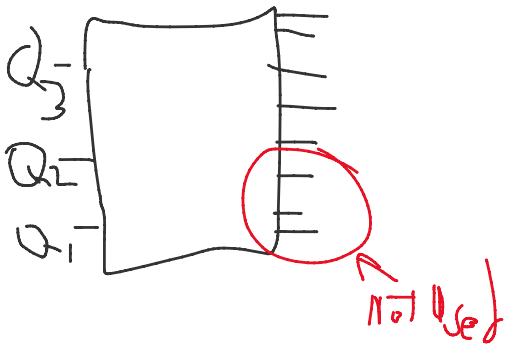
Day 5 (Jan 31st)

Sunday, February 2, 2020 2:11 AM

Mod 5 Counter





Q_3	Q_2	Q_1		Q_3^+	Q_2^+	Q_1^+
0	0	0	|	0	0	1
0	0	1	|	0	1	0
0	1	0	|	0	1	1
0	1	1	|	1	0	0
1	0	0	|	0	0	0
1	0	1	|	X **(0)**	X **(1)**	X **(0)**
1	1	0	|	X **(0)**	X **(1)**	X **(0)**
1	1	1	|	X **(1)**	X **(0)**	X **(0)**

Same Problem

Q_3^+:

			Q_2	Q_2	
	0	0	1	0	
Q_3	0	X	X	X	
		Q_1	Q_1		

$Q_3^+ = Q_1Q_2$

Make Sure to go back into the truth table and fill in the don't cares

Q_2^+:

			Q_2	Q_2	
	0	1	0	1	
Q_3	0	X	X	X	
		Q_1	Q_1		

$Q_2^+ = Q_1Q_2' + Q_2Q_1'$ <- That is Exclusive Or

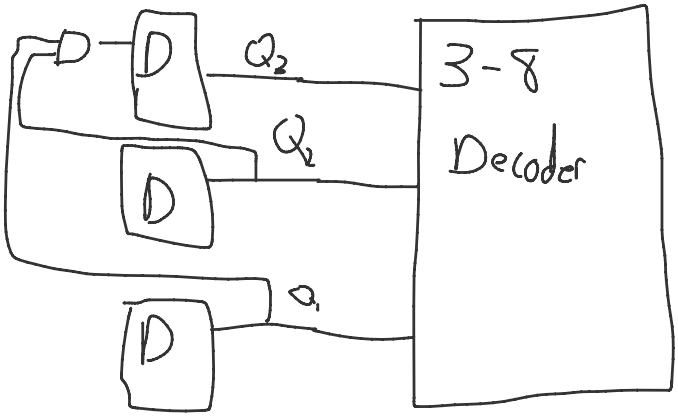
Make Sure to go back into the truth table and fill in the don't cares

Q_1^+:

			Q_2	Q_2	
	1	0	0	1	
Q_3	0	X	X	X	
		Q_1	Q_1		

$Q_1^+ = Q_3'Q_1'$

Make Sure to go back into the truth table and fill in the don't cares



These Circuits are **Self Correcting** (Even the don't care states push to a valid state without an infinite loop.

I_D	Q
0	0
1	1

Input D Flip Flop = I_D
Input T Flip Flop = I_T

I_T	Q
0	No Change
1	Complement

Q_3	Q_2	Q_1	|	Q_3^+	Q_2^+	Q_1^+	|	I_{T3}^+	I_{T2}^+	I_{T1}^+	|	Q_{T3}^+	Q_{T2}^+	Q_{T1}^+
0	0	0	|	0	0	1	|	0	0	1	|	0	0	1
0	0	1	|	0	1	0	|	0	1	1	|	0	1	0
0	1	0	|	0	1	1	|	0	0	1	|	0	1	1
0	1	1	|	1	0	0	|	1	1	1	|	1	0	0
1	0	0	|	0	0	0	|	1	0	0	|	0	0	0
1	0	1	|	X **(0)**	X **(1)**	X **(0)**	|	X **(1)**	X **(1)**	X **(0)**	|	0	1	1
1	1	0	|	X **(0)**	X **(1)**	X **(0)**	|	X **(1)**	X **(0)**	X **(0)**	|	0	1	0
1	1	1	|	X **(1)**	X **(0)**	X **(0)**	|	X **(0)**	X **(1)**	X **(0)**	|	1	0	1

I_{T3}^+:

			Q_2	Q_2	
	0	0	1	0	
Q_3	1	X	X	X	
		Q_1	Q_1		

$I_{T3}^+ = Q_3+Q_1Q_2$
Make Sure to go back into the truth table and fill in the don't cares

I_{T2}^+:

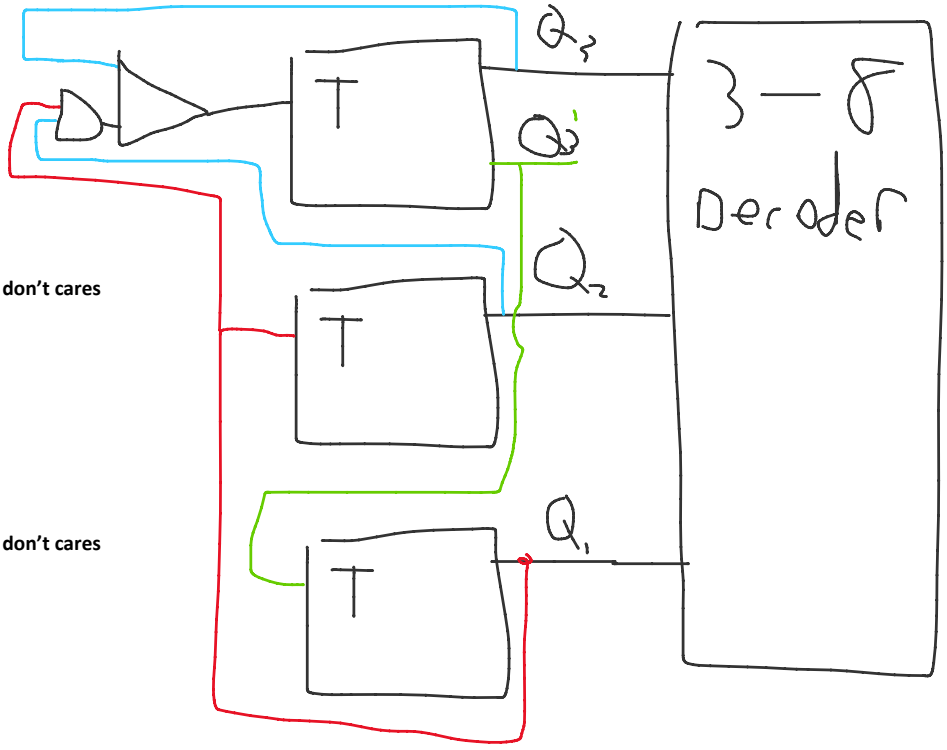
			Q_2	Q_2	
	0	1	1	0	
Q_3	0	X	X	X	
		Q_1	Q_1		

$I_{T2}^+ = Q_1$
Make Sure to go back into the truth table and fill in the don't cares

I_{T1}^+:

			Q_2	Q_2	
	1	1	1	1	
Q_3	0	X	X	X	
		Q_1	Q_1		

$I_{T1}^+ = Q_3'$
Make Sure to go back into the truth table and fill in the don't cares



Multiplication:

Multiplication in the ALU takes multiple clock cycle
Signed and Unsigned are separate circuits in Multiplication

Step	C (Carry) (1 bit)	A (Answer) (4 bit)	Q (Multiplier) (4 bit)	M (First Number) (4 bit)	Operation
0	0	0000	1011	1101	Initialize
1	0	1101	1011	1101	Add M to A (0000 + 1101=

					01101)
1.5	0	0110	1101	1101	Shift
2	1	0011	1101	1101	Add M to A (0110 + 1101= 10011)
2.5	0	1001	1110	1101	Shift
3	0	1001	1110	1101	Add Zero to A (0000 + 1001=01001)
3.5	0	0100	1111	1101	Shift
4	1	0001	1111	1101	Add M to A (1101 + 0100 = 10001)
4.5	0	1000	1111	1101	Shift

So Row 4.5 is the answer A_Q makes 10001111b = 143
1101 = 13
1011 = 11
13 * 11 = 143 So We are correct