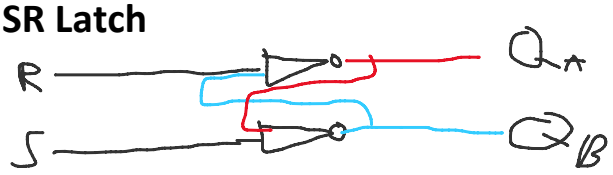
Day 4 (Jan 29th)

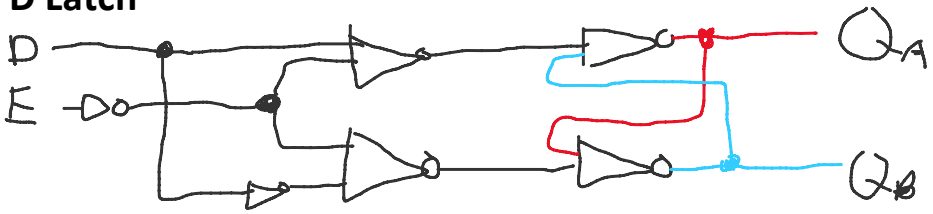
Sunday, February 2, 2020 2:11 AM

SR Latch



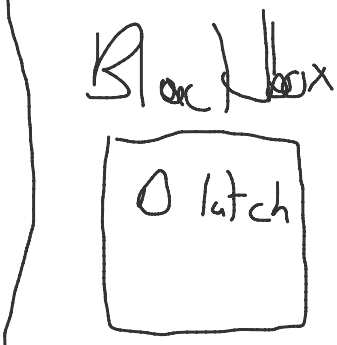
S	R		Q_a	Q_b
0	0	|	No Change	No Change
0	1	|	0	1
1	0	|	1	0
1	1	|	Prevent This	Prevent This

D Latch



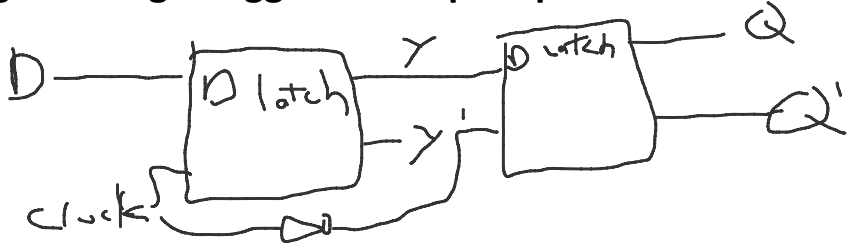
E Stands For Enable
D Stands For Data

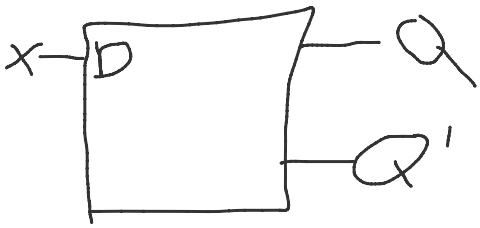
E	D		Q_a	Q_b
0	X	|	NC	NC
1	0	|	0	1
1	1	|	1	0



Clock Cycle Negative Edge

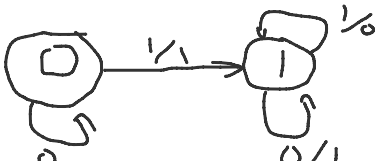
Negative Edge Triggered D Flip-Flop





8 Of these together forms an 8 bit register

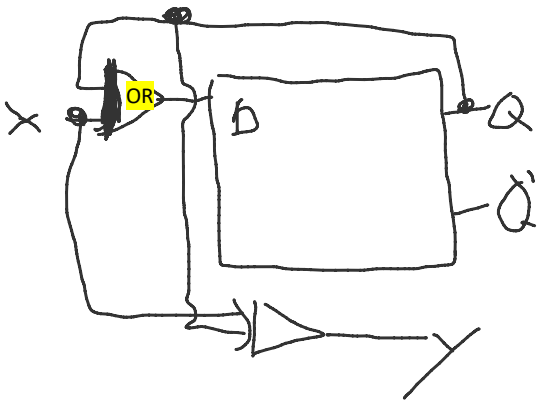
Sequential 2s Complementor



Input / output

Q_t	X	|	Q_{t+1}	Y
0	0	|	0	0
0	1	|	1	1
1	0	|	1	1
1	1	|	1	0

Q_{t+1}: Q_t+x
Y: $Q_t \oplus x$
$\oplus$ means exclusive or



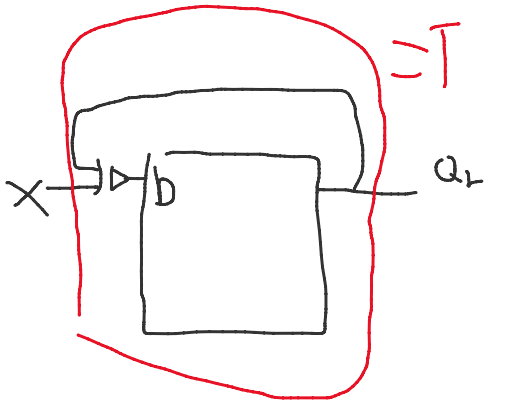
D Flip-Flop

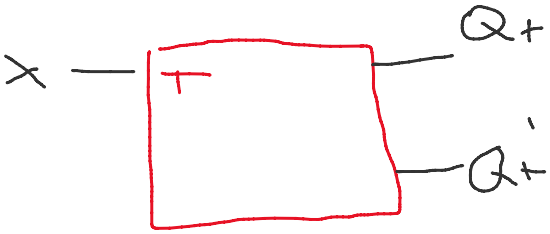
X	Q
0	0
1	1

T Flip-Flop

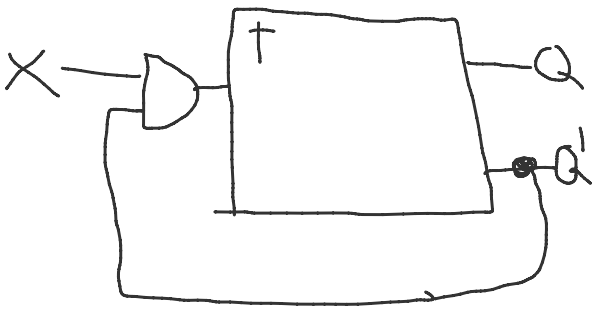
X	Q
0	No Change
1	Complement

Q_t	X	|	Q_{t+1}
0	0	|	0
0	1	|	1
1	0	|	1
1	1	|	0





			D Flip-	Flop		T Flip-Flop
Q_t	X	|	Q_{t+1}	Y	|	I_T
0	0	|	0	0	|	0
0	1	|	1	1	|	1
1	0	|	1	1	|	0
1	1	|	1	0	|	0



Going back to the 2s Complementor, it was simpler to use the D flip flop version than the T Version